SCIENCE
PASSION
TECHNOLOGY

Lightweight Block-Level Formal Verification

A Graphical Guide

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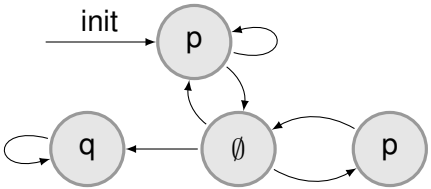
Interests FPGA architectures
FPGA backend flows
Applied formal verification

My Initial View on Formal Verification

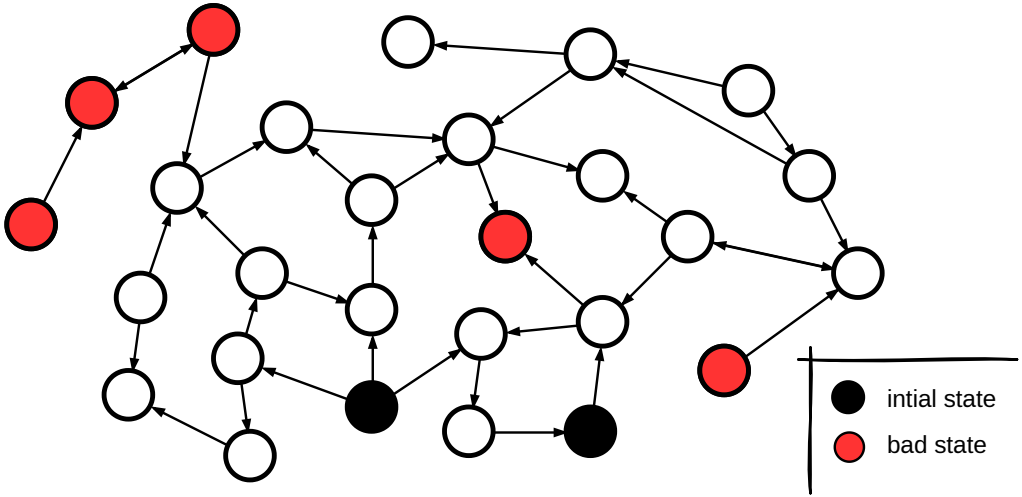
- **Kripke structure**
- $M = (S, S_0, R, AP, L)$
- $M, s \overset{?}{\models} \square(p \rightarrow \neg \bigcirc q)$
- ...



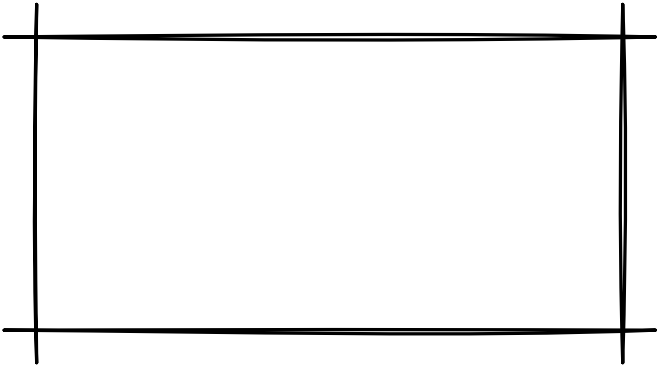
"not practical" $\longrightarrow$ preferred verification method for *suitable* designs

What is this presentation (not) about?

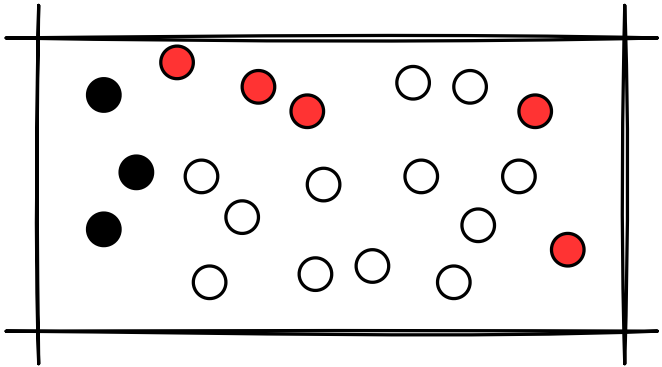
- ⊕ Practical application
- ⊕ Graphical
- ⊕ Designer's guide
- ⊖ Theoretical background
- ⊖ Tools, languages, ...



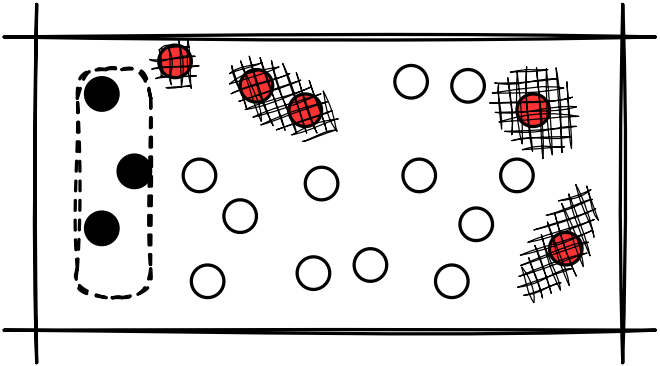
See also [12, 13]



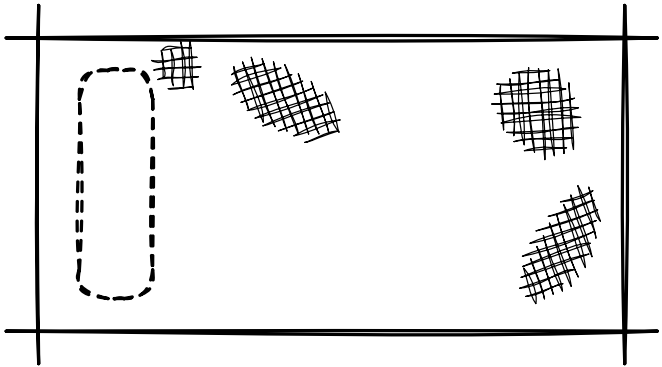
Partly adapted from [8]



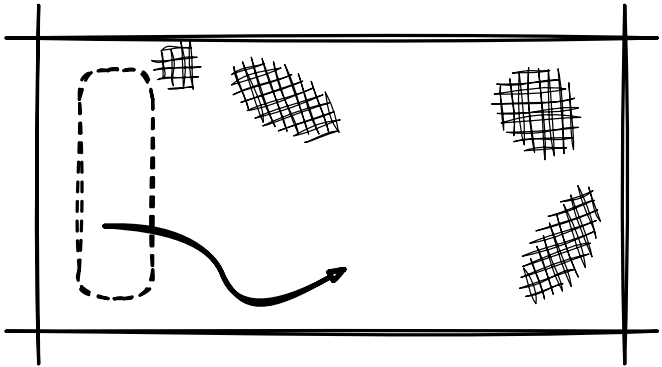
Partly adapted from [8]



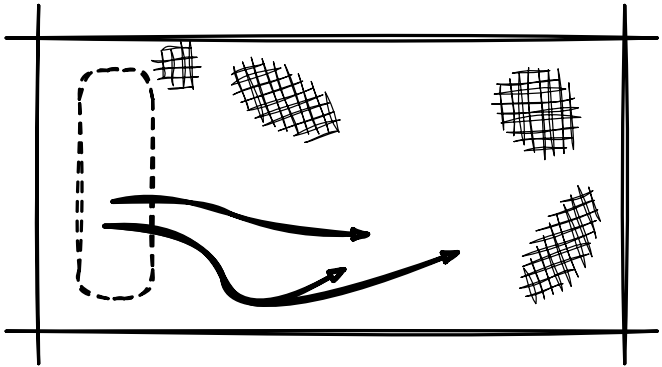
Partly adapted from [8]



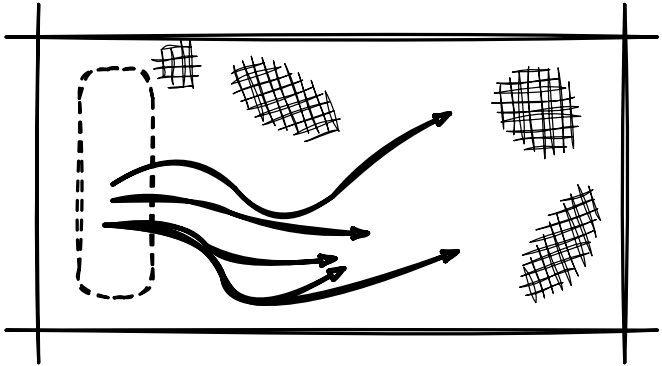
Partly adapted from [8]



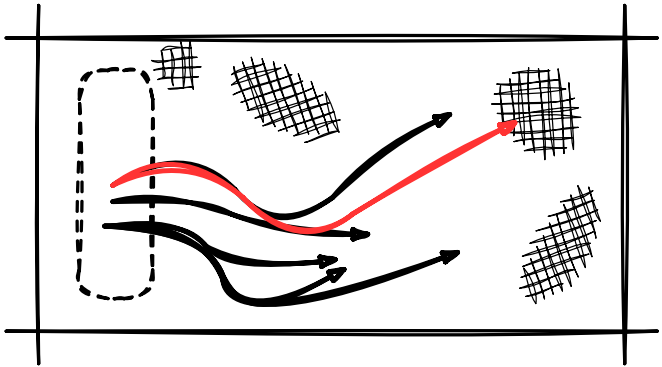
Partly adapted from [8]



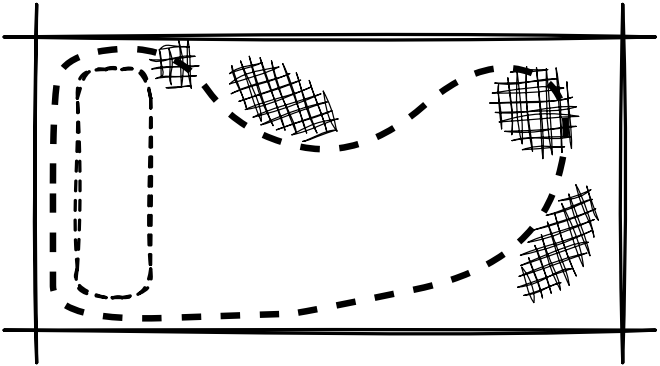
Partly adapted from [8]



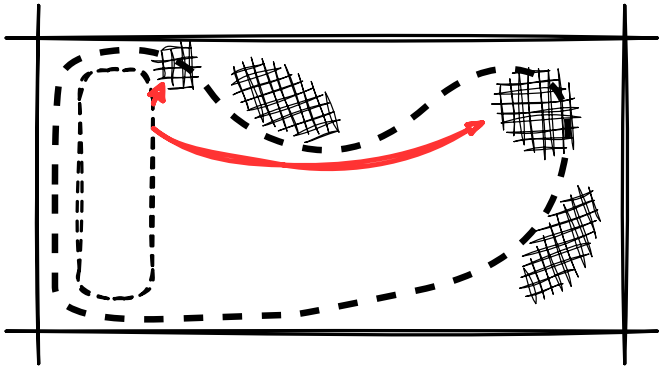
Partly adapted from [8]



Partly adapted from [8]



Partly adapted from [8]

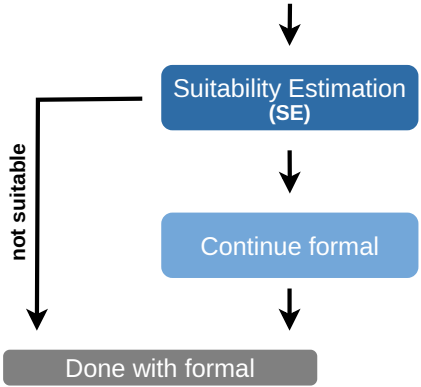


Partly adapted from [8]

Methodology [7]

- For designers
- Formalize the endeavor
- Concise
- Lightweight

Design Suitable for Formal?



Suitability Estimation (SE)

- ⊕ Control-oriented designs
- ⊕ Data transportation
- ⊖ (Deep) sequential designs
- ⊖ Data transformation

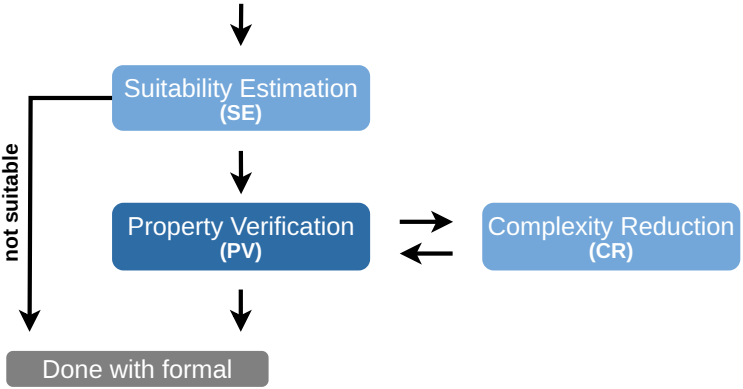
Based on [2, 3]

Formal Friendly Designs

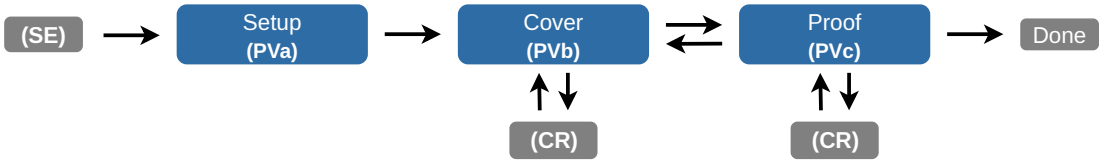
- ⊕ Arbiters, scheduler
- ⊕ DMA controller
- ⊕ Interrupt controller
- ⊖ Floating point unit
- ⊖ Convolution unit
- ⊖ Graphics shader

Based on [2, 3]

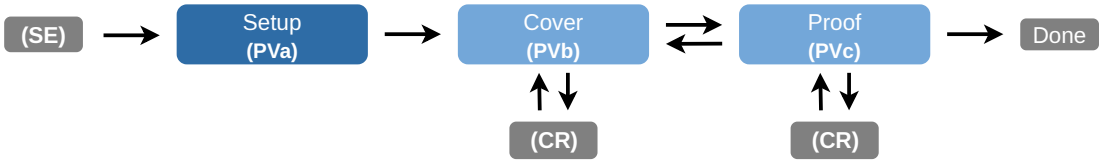
Continue Formal Endeavor



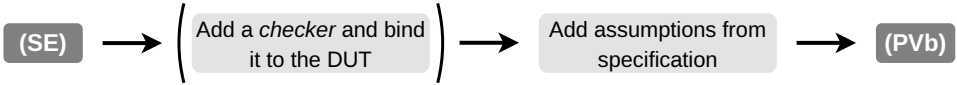
Property Verification (PV)



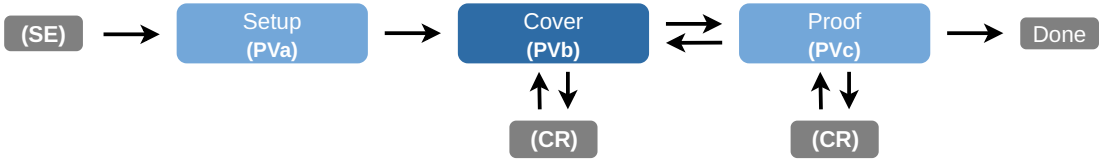
Property Verification (PV)

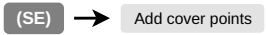


Setup (PVa)

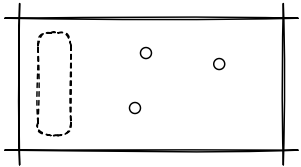

(SE)
Add a *checker* and bind it to the DUT
Add assumptions from specification
(PVb)

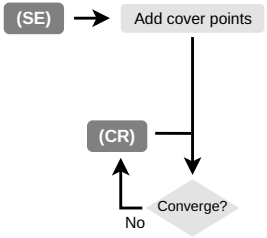
Property Verification (PV)

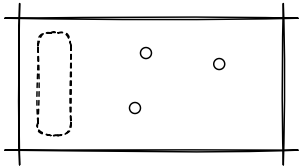


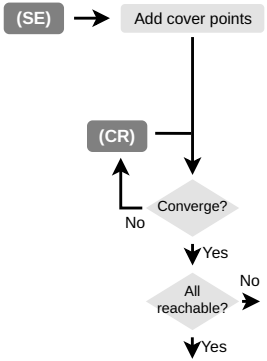

(SE)
Add cover points

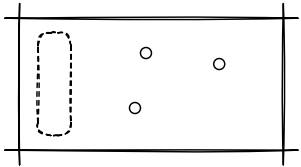
(SE) → Add cover points

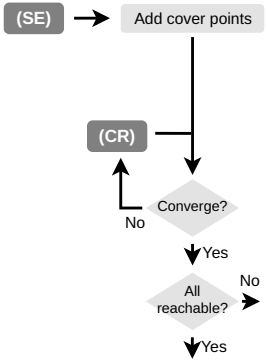


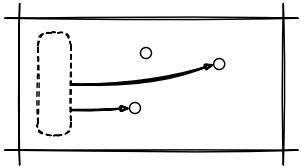

(SE)
Add cover points
(CR)
Converge?
No

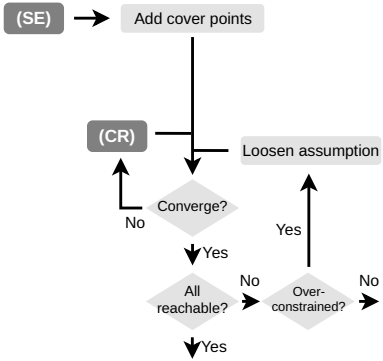


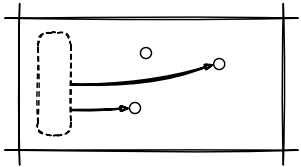

(SE)
Add cover points
(CR)
Converge?
No
Yes
All reachable?
No
Yes

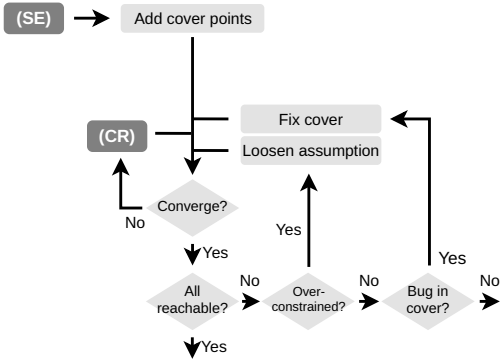


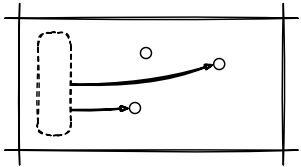

(SE)
Add cover points
(CR)
Converge?
No
Yes
All reachable?
No
Yes

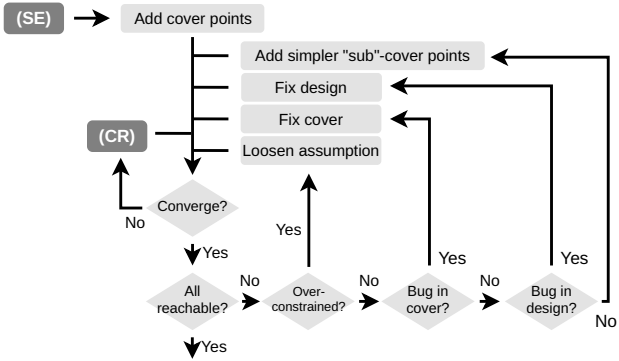


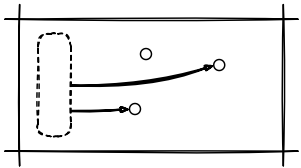

(SE)
Add cover points
(CR)
Loosen assumption
Converge?
No
Yes
All reachable?
No
Over-constrained?
No
Yes
Yes

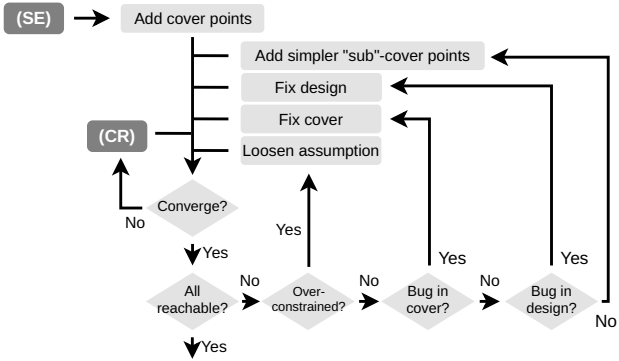


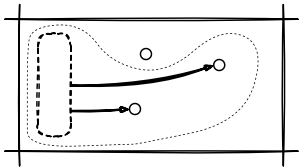

(SE)
Add cover points
(CR)
Fix cover
Loosen assumption
Converge?
No
Yes
All reachable?
No
Yes
Over-constrained?
No
Yes
Bug in cover?
No
Yes

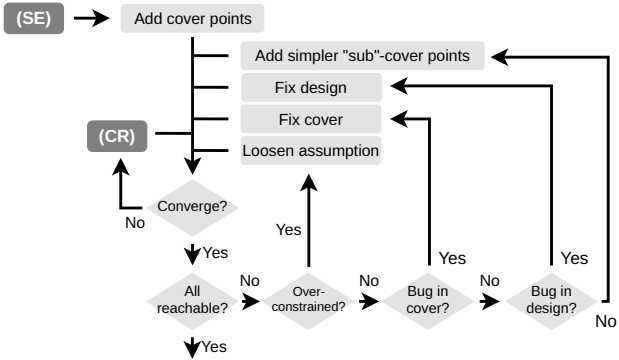


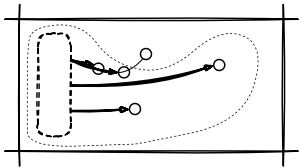

(SE)
Add cover points
Add simpler "sub"-cover points
Fix design
Fix cover
Loosen assumption
(CR)
Converge?
No
Yes
All reachable?
No
Yes
Over-constrained?
No
Yes
Bug in cover?
No
Yes
Bug in design?
No
Yes

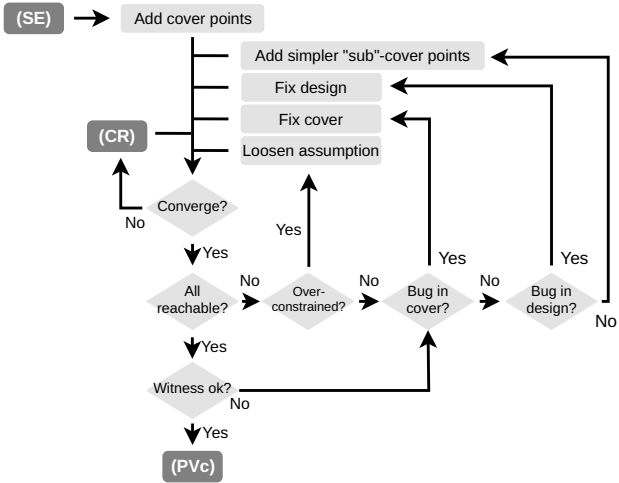


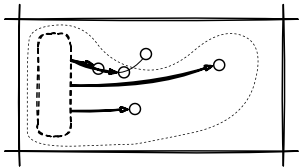

(SE)
Add cover points
Add simpler "sub"-cover points
Fix design
Fix cover
Loosen assumption
(CR)
Converge?
No
Yes
All reachable?
No
Yes
Over-constrained?
No
Yes
Bug in cover?
No
Yes
Bug in design?
No
Yes



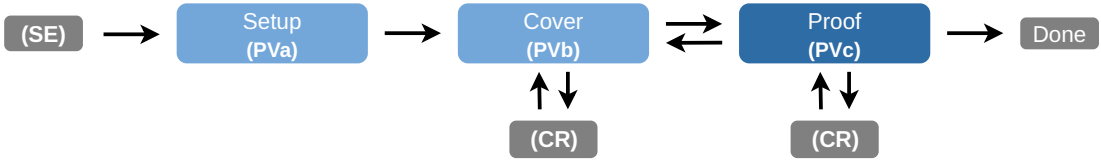

(SE)
Add cover points
Add simpler "sub"-cover points
Fix design
Fix cover
Loosen assumption
(CR)
Converge?
No
Yes
All reachable?
No
Yes
Over-constrained?
No
Yes
Bug in cover?
No
Yes
Bug in design?
No
Yes

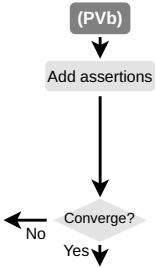


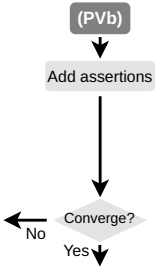

(SE)
Add cover points
Add simpler "sub"-cover points
Fix design
Fix cover
Loosen assumption
(CR)
Converge?
No
Yes
All reachable?
No
Over-constrained?
No
Bug in cover?
No
Bug in design?
No
Yes
Yes
Yes
Yes
Witness ok?
No
Yes
(PVc)

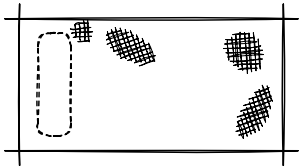


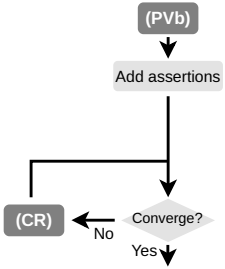
Property Verification (PV)

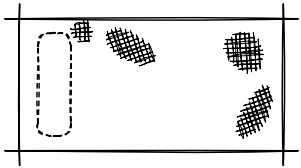


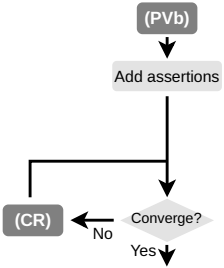

(PVb)
Add assertions
Converge?
No
Yes

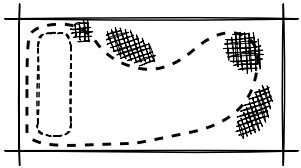

(PVb)
Add assertions
Converge?
No
Yes

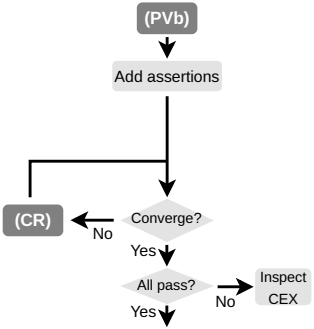


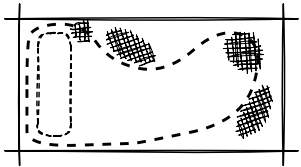

(PVb)
Add assertions
(CR)
No
Converge?
Yes

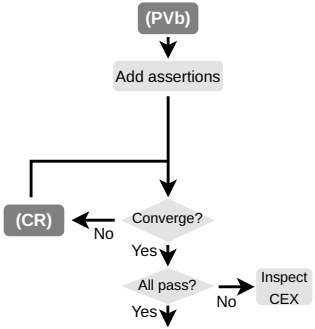


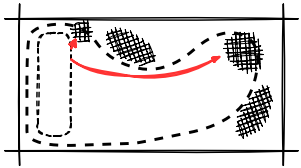

(PVb)
Add assertions
(CR)
No
Converge?
Yes

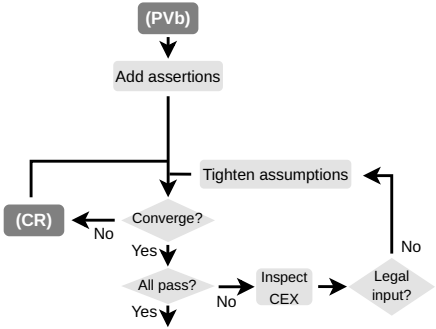


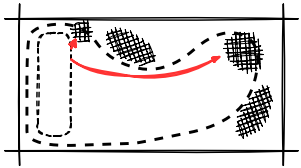

(PVb)
Add assertions
(CR)
No
Converge?
Yes
All pass?
No
Inspect CEX
Yes

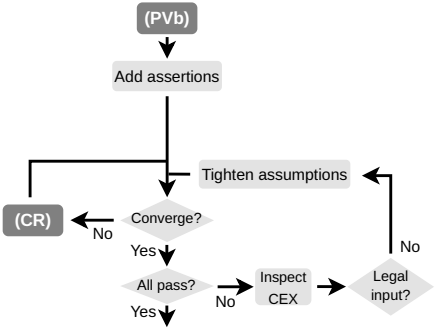


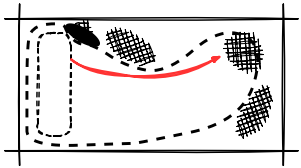

(PVb)
Add assertions
(CR)
No
Converge?
Yes
All pass?
No
Inspect CEX
Yes

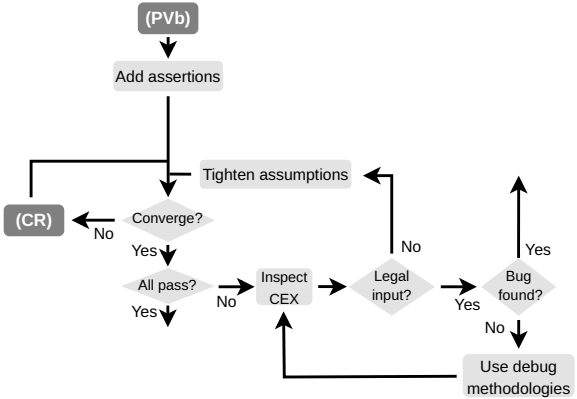


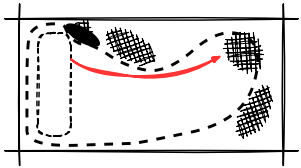

(PVb)
Add assertions
Tighten assumptions
(CR)
No
Converge?
Yes
All pass?
No
Inspect CEX
Legal input?
No
Yes

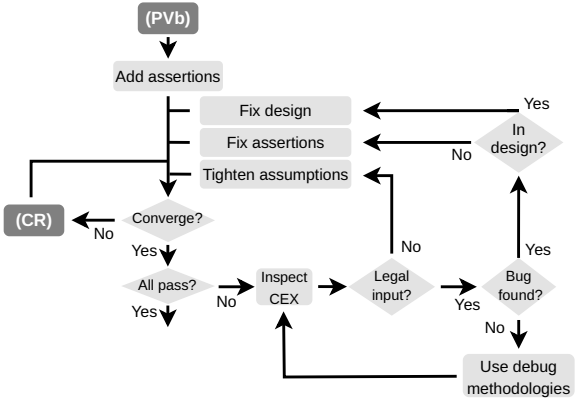


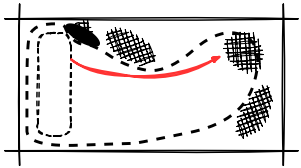

(PVb)
Add assertions
Tighten assumptions
(CR)
No
Converge?
Yes
All pass?
No
Inspect CEX
Legal input?
No
Yes

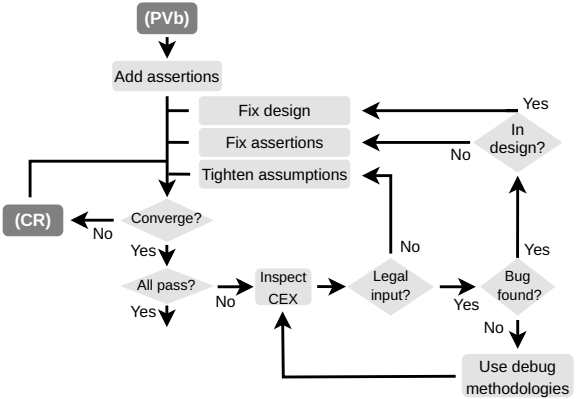


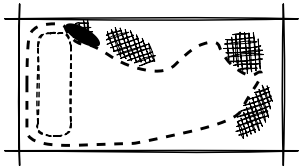

(PVb)
Add assertions
Tighten assumptions
(CR)
Converge?
No
Yes
All pass?
Yes
No
Inspect CEX
Legal input?
No
Yes
Bug found?
Yes
No
Use debug methodologies

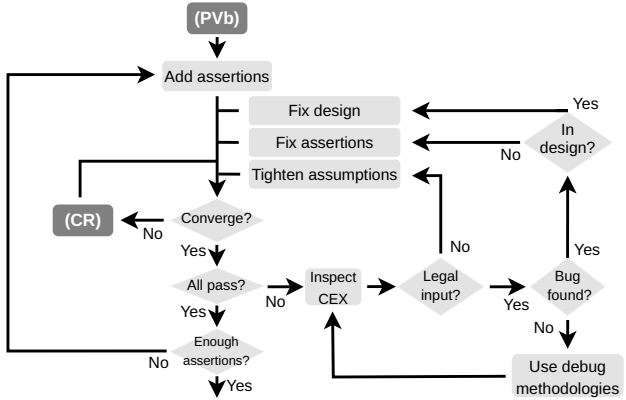


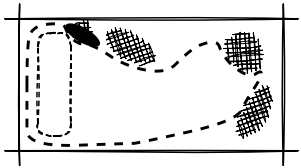

(PVb)
Add assertions
Fix design
Fix assertions
Tighten assumptions
Yes
In design?
No
(CR)
Converge?
No
Yes
All pass?
No
Yes
Inspect CEX
Legal input?
No
Yes
Bug found?
Yes
No
Use debug methodologies

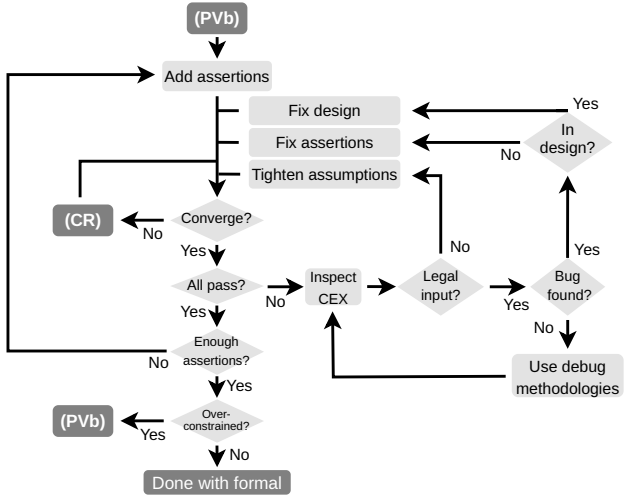


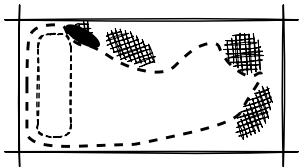

(PVb)
Add assertions
Fix design
Fix assertions
Tighten assumptions
(CR)
Converge?
No
Yes
All pass?
Yes
No
Inspect CEX
Legal input?
No
Yes
In design?
Yes
No
Bug found?
Yes
No
Use debug methodologies




(PVb)
Add assertions
Fix design
Fix assertions
Tighten assumptions
(CR)
Converge?
No
Yes
All pass?
No
Yes
Enough assertions?
No
Yes
Inspect CEX
Legal input?
No
Yes
Bug found?
Yes
No
In design?
Yes
No
Use debug methodologies




(PVb)
Add assertions
Fix design
Fix assertions
Tighten assumptions
(CR)
Converge?
No
Yes
All pass?
No
Yes
Inspect CEX
Legal input?
No
Yes
In design?
Yes
No
Bug found?
Yes
No
Use debug methodologies
Enough assertions?
No
Yes
(PVb)
Over-constrained?
Yes
No
Done with formal



Complexity Reduction (CR)

- Highly application specific
- See [1, 8, 3, 2, 4, 5, 10]

Complexity Reduction (CR)

Property Optimization

- Efficient property design
- Auxiliary code
- Assumption optimization

Complexity Reduction (CR)

Abstraction

- Parameter optimization
- Cut-points
- Black-boxing
- Shadow modeling

Complexity Reduction (CR)

Tool Specific & Strategy

- Different engine
- Bounded proof
- Continue with simulation

(Open-Source) Examples

- YosysHQ Read the Docs (great starting point) [14, 17]
- `YosysHQ/sby` [16]
- `riscv-formal` [15]
- The Tiny Tapeout Multiplexer [11]

SystemVerilog Assertions

- SystemVerilog Assertions Basics [9]
- SystemVerilog LRM [6]
- SVA: The Power of Assertions in SystemVerilog [1]
- Formal Verification: An Essential Toolkit for Modern VLSI Design [8]
- Open source support?

www.meinhard-kissich.at/pub/orconf23_slides.pdf

www.meinhard-kissich.at

meinhard.kissich@tugraz.at

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