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System-on-Chip Design: From Requirements to ASIC

Open-Source, Optimized, and Human-out-of-the-Loop

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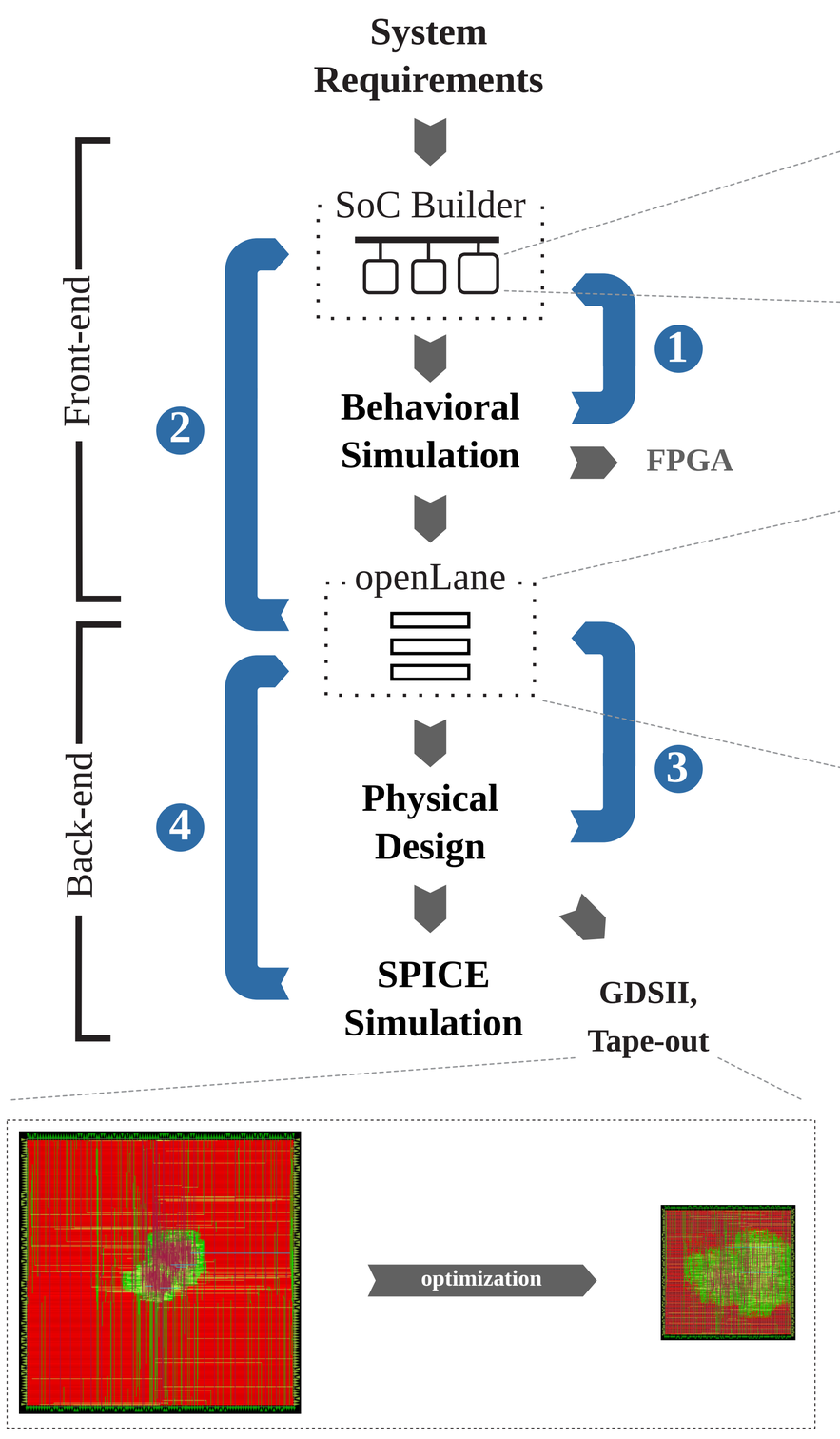
Abstract

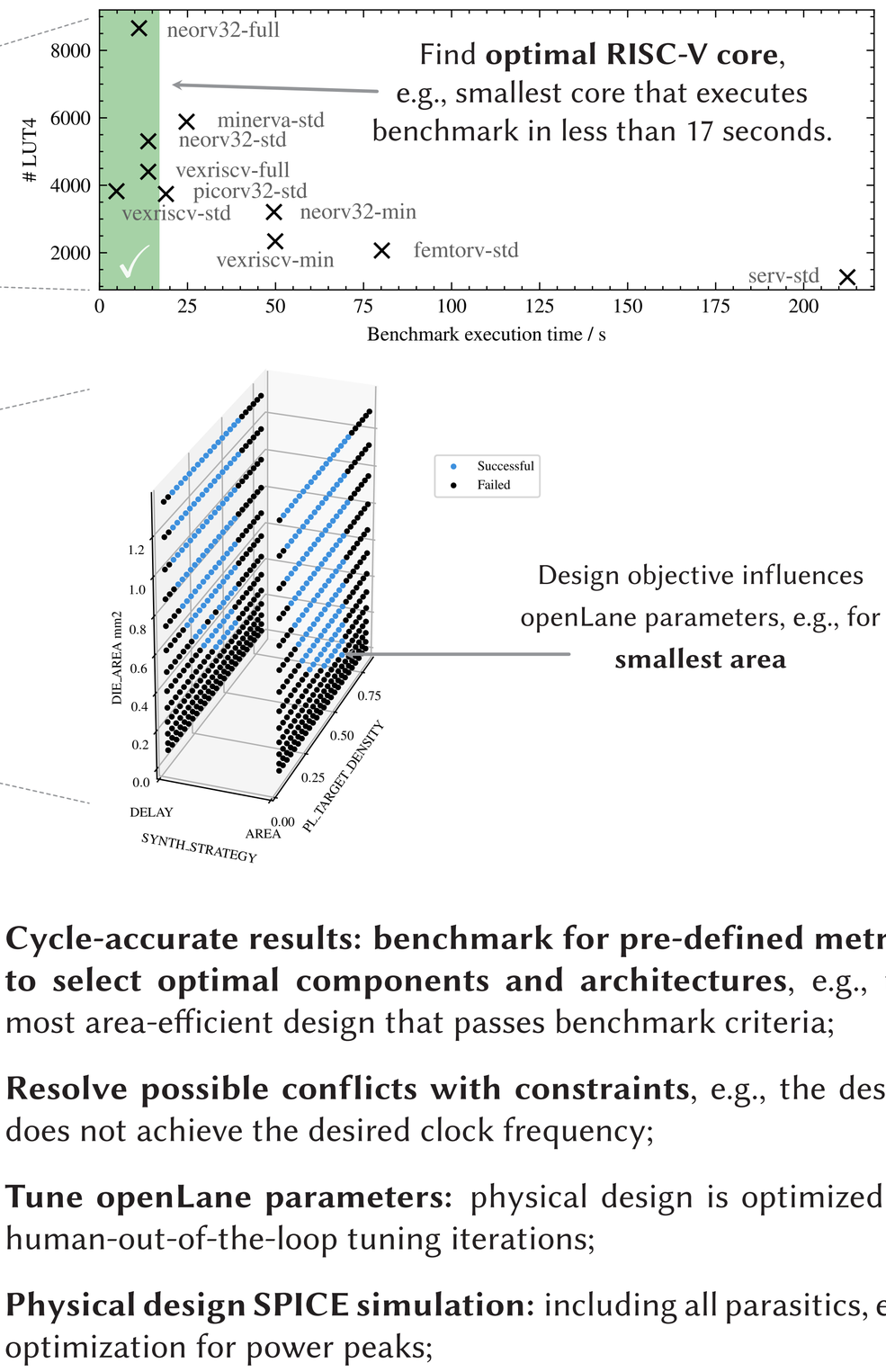
Heterogeneous embedded systems tailored to the target use case became increasingly important to cope with tight performance, power, and cost constraints. System architecture and decisions in digital design considerably impact these metrics. However, synthesis and the physical design influences should not be underestimated. While Electronic Design Automation (EDA) tools have been proprietary in the past, there is a strong push toward open-source silicon with a high potential for research and innovation. In conjunction with processing cores based on the RISC-V instruction set architecture, highly customized and open-source System-on-Chip (SoC) designs are achievable and reproducible by everyone throughout all stages. We work on a flow to optimize and automate SoC design, from selecting components, through building the SoC, to parameter tuning in the backend by a human-out-of-the-loop approach.

Situation & Opportunities

- Rising number of embedded and connected devices with substantially diverging requirements
  - ↪ Towards push-button flow: *Requirements → SoC design*
- Tight constraints on energy and power consumption, cost, time-to-market, ...
  - ↪ Benefit from a diverse set of open-source RISC-V cores
  - ↪ Optimize for the target use case in front-end and back-end
- Established EDA tools are proprietary, cost-intensive, restrictive
  - ↪ Open Verilog-to-GDSII ASIC flow, open SkyWater130 PDK
  - ↪ Active research, permitted to publish all artifacts

Flow





1. **Cycle-accurate results: benchmark for pre-defined metrics to select optimal components and architectures**, e.g., the most area-efficient design that passes benchmark criteria;
2. **Resolve possible conflicts with constraints**, e.g., the design does not achieve the desired clock frequency;
3. **Tune openLane parameters:** physical design is optimized by human-out-of-the-loop tuning iterations;
4. **Physical design SPICE simulation:** including all parasitics, e.g., optimization for power peaks;

Want to get Involved?

An end-to-end flow from requirements to ASIC tape-out can benefit from cross-domain collaborations and demands expertise in various fields: system architecture, digital design, low-level software, EDA tools, electronic simulation, optimization, and machine learning, to name a few. If you are interested in getting involved, do not hesitate to contact us.

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